

REMARKS

Summary of Office Action

Claims 1, 3-8, 10-12, 14-16, 20-22, 24, 26-28, 30 and 32-44 are pending in this application.

Claims 1, 3-7, 26, 33, 38 and 41 have been rejected under 35 U.S.C. § 103(a) as being obvious from Gorecki U.S. Patent Application Publication No. 2004/0071205 ("Gorecki") in view of WinSLAC Software User's Guide (1999) ("WinSLAC") and Altera Corporation, "FIR Compiler MegaCore Function" ("Solution Brief 41"). Claims 21, 22, 30 and 36 have been rejected under 35 U.S.C. § 103(a) as being obvious from Jaynes et al. U.S. Patent Application Publication No. 2005/0047779 ("Jaynes") in view of WinSLAC and Solution Brief 41. Claims 20, 40 and 44 have been rejected under 35 U.S.C. § 103(a) as being obvious from Jaynes in view of WinSLAC, Solution Brief 41 and Hillery U.S. Patent No. 6,178,201 ("Hillery"). Claims 8, 10, 11, 24, 27, 32, 34, 37, 39 and 42 have been rejected under 35 U.S.C. § 103(a) as being obvious from Gorecki and Lu U.S. Patent No. 6,275,836 ("Lu") in view of WinSLAC and Solution Brief 41. Claims 12, 14, 15, 28 and 35 have been rejected under 35 U.S.C. § 103(a) as being obvious from Pederson et al. U.S. Patent Application Publication No. 2006/0114979 ("Pederson") in view of WinSLAC and Solution Brief 41. Claims 16 and 43 have been rejected under 35 U.S.C. § 103(a) as being obvious from Pederson in view of WinSLAC, Solution Brief 41 and Gorecki.

Applicants' Reply

Claims 1, 3-7, 26, 33, 38 and 41

Claims 1, 3-7, 26, 33, 38 and 41 have been rejected under 35 U.S.C. § 103(a) as being obvious from Gorecki in view of WinSLAC and Solution Brief 41. This rejection is respectfully traversed.

Applicants' invention, as defined by claims 1 and 26, is directed to receiver circuitry and methods for adaptively equalizing a data signal. The receiver circuitry and methods include, *inter alia*, programmable circuitry that is programmed with a first value corresponding to a first number of taps. Processing circuitry computes a second value corresponding to a second number of taps. Selection circuitry selects one of the first and second values at the time the programmable circuitry is being programmed by configuration data.

Solution Brief 41 discusses a FIR compiler wizard (software) that allows a user to create FIR filters. The software displays one selectable option to have filter coefficients provided from a file and a second option to have the coefficients generated by the compiler. The response of the filter can be viewed dynamically as the coefficient settings are changed. The wizard outputs code that can be used to synthesize FIR filters of hardware architectures. (Solution Brief 41, FIG. 2 and pages 1 and 2.)

The Examiner acknowledges that Gorecki and WinSLAC fail to show or suggest selection circuitry that selects based on a control signal one of a first value that is programmed and second value that is computed and cites Solution Brief 41 as

allegedly making up for this deficiency (Office Action, page 4). Applicants respectfully disagree and submit that Gorecki, WinSLAC and Solution Brief 41, alone or in combination, do not show or suggest selection circuitry that selects a first value that is programmed and a second value that is computed at the time the programmable circuitry is being programmed by configuration data, as defined by applicants' claims 1 and 26.

First, applicants respectfully submit that because Solution Brief 41 discloses a software tool that can be used to model various filter behavior and generate files to create a particular filter having the desired taps and coefficients, Solution Brief 41 fails to show or suggest an already implemented receiver circuitry with selection circuitry. More specifically, the mere simulation and generation of files of receiver circuitry, as discussed in Solution Brief 41, is not the same as a circuit that is implemented to perform a particular function (e.g., select between two values), as defined by applicants' claims. In particular, Solution Brief 41 allows the user to select whether coefficient values are provided by a file or generated by the compiler in order to simulate and synthesize (implement) a filter with a desired behavior. However, once the filter with the desired behavior is synthesized (implemented), the filter does not select between user provided coefficient values and compiler generated coefficient values as this selection is only performed during the simulation of the filter. Indeed, the compiler wizard (which allows such selection and generates the alleged computed

values) is not implemented in the filter and thus cannot provide the alleged computed coefficient values to the alleged selection circuitry in the implemented filter.

Second, Solution Brief 41 discusses the user selecting whether the coefficient values are read from a file (i.e., the alleged first value) or generated using the compiler (i.e., the alleged second value) by selecting respective options from a display. Therefore, Solution Brief 41 necessarily does not show or suggest that the selection, between the first and second values, that is made by the circuitry is based on a control signal.

Finally, even if the user were analogized with selection circuitry that selects based on a control signal, Solution Brief 41 would still fail to show or suggest selection circuitry that selects one of two values at the time the programmable circuitry is being programmed by configuration data, as required by applicants' claims 1 and 26. In particular, in Solution Brief 41 the selection between the alleged two values is made while simulating the behavior of the filter and before a configuration file of the filter is created. Therefore, because the alleged selection is made prior to the existence of the configuration data (i.e., before the compiler outputs the simulation file), the alleged selection is necessarily not made at the time the programmable circuitry is being programmed by configuration data.

Thus, Solution Brief 41 does not make up for the deficiencies of Gorecki and WinSLAC relative to the rejection. Therefore, Gorecki and WinSLAC, whether taken alone or in

combination, do not show or suggest all the features of applicants' claims 1 and 26. Accordingly, applicants respectfully submit that independent claims 1 and 26 and claims 3-7, 33, 38 and 41 that depend, directly or indirectly from claim 1 or 26, are allowable.

Claims 8, 10, 11, 27, 34, 39 and 42

Claims 8, 10, 11, 27, 34, 39 and 42 have been rejected under 35 U.S.C. § 103(a) as being obvious from Gorecki and Lu in view of WinSLAC and Solution Brief 41. This rejection is respectfully traversed.

Applicants' invention, as defined by independent claims 8 and 27, is directed to receiver circuitry and methods for adaptively equalizing a data signal. The receiver circuitry and methods include, *inter alia*, programmable circuitry that is programmed with a first value indicating a first selection between integer spacing and fractional spacing of the taps. Processing circuitry computes a second value indicating a first selection between integer spacing and fractional spacing of the taps. Selection circuitry selects one of the first and second values at the time the programmable circuitry is being programmed by configuration data.

The Examiner acknowledges that Gorecki and WinSLAC fail to show or suggest selection circuitry that selects one of the first and second values based on a control signal and relies on Solution Brief 41 to make up for this deficiency (Office Action, pages 10-12).

As discussed above with respect to claims 1 and 26, applicants respectfully submit that Solution Brief 41 does not show or suggest selection circuitry that selects one of two values based on a control signal at the time the programmable circuitry is being programmed by configuration data. Thus, Solution Brief 41 does not show or suggest these features defined by applicants' claims 8 and 27.

Lu does not make up for the deficiencies of Gorecki, WinSLAC and Solution Brief 41 relative to the rejection.

Therefore, Gorecki, WinSLAC, Solution Brief 41 and Lu, whether taken alone or in combination, do not show or suggest all the features of applicants' claims 8 and 27. Accordingly, applicants respectfully submit that independent claims 8 and 27 and claims 10, 11, 34, 39 and 42 that depend, directly or indirectly from claim 8 or 27, are allowable.

Claims 12, 14-16, 28, 35 and 43

Claims 12, 14, 15, 28 and 35 have been rejected under 35 U.S.C. § 103(a) as being obvious from Pederson in view of WinSLAC and Solution Brief 41. Claims 16 and 43 have been rejected under 35 U.S.C. § 103(a) as being obvious from Pederson in view of WinSLAC, Solution Brief 41 and Gorecki. These rejections are respectfully traversed.

Applicants' invention, as defined by independent claims 12 and 28, is directed to receiver circuitry and methods for adaptively equalizing a data signal. The receiver circuitry and methods include, inter alia, programmable circuitry that is programmed with a first starting value and

outputs the first starting value and a control signal. Processing circuitry computes a second starting value and outputs the second starting value in parallel with the first starting value. Selection circuitry receives the control signal and the first and second starting values in parallel and selects one of the first and second starting values based on the control signal at the time the programmable circuitry is being programmed by configuration data.

Applicants respectfully submit that Penderson does not show or suggest programmable circuitry that is programmed by configuration data, as defined by applicants' claims 12 and 28. In particular, the Examiner alleges that a bank of settings available to the user in Penderson is the same as applicants' claimed programmable circuitry (Office Action, page 15). However, contrary to the Examiner's allegations, nowhere does Penderson show or suggest that the bank of settings is programmed by configuration data. Moreover, Penderson discloses the bank of settings being made available to the user (and perhaps modified by the user) which is not the same as programming the bank of settings with configuration data. WinSLAC and Solution Brief 41 were cited as showing other features of applicants' claims and do not make up for the deficiencies of Penderson in that regard.

In addition, the Examiner acknowledges that Pederson and WinSLAC fail to show or suggest selection circuitry that receives the first and second training patterns in parallel and selects one of the first and second values based on a control

signal and relies on Solution Brief 41 to make up for this deficiency (Office Action, page 15).

As discussed above with respect to claims 1, 8, 26 and 27, Solution Brief 41 does not show or suggest selection circuitry that selects one of two values based on a control signal. Thus, Solution Brief 41 does not show or suggest these features defined by applicants' claims 12 and 28.

Therefore, Penderson, WinSLAC and Solution Brief 41, whether taken alone or in combination, do not show or suggest all the features of applicants' claims 12 and 28. Accordingly, applicants respectfully submit that claims 12 and 28, and claims 14-16, 35 and 43 that depend, directly or indirectly, from claim 12 or 28, are allowable.

Claims 21, 22, 30 and 36

Claims 21, 22, 30 and 36 have been rejected under 35 U.S.C. § 103(a) as being obvious from Jaynes in view of WinSLAC and Solution Brief 41. This rejection is respectfully traversed.

Applicants' invention, as defined by claims 22 and 30, is directed to receiver circuitry and a method for adaptively equalizing a data signal. The receiver circuitry and methods include, *inter alia*, programmable circuitry that is programmed with a first training pattern and outputs the first training pattern and a first control signal. Training pattern circuitry stores a second training pattern and outputs the second training pattern in parallel with the first training pattern. Selection circuitry receives the first control signal

and the first and second training patterns in parallel and selects one of the first and second training pattern based on the first control signal at the time the programmable circuitry is being programmed by configuration data.

The Examiner acknowledges that Jaynes and WinSLAC fail to show or suggest selection circuitry that receives the first and second training patterns in parallel and selects one of the first and second values based on a control signal and relies on Solution Brief 41 to make up for this deficiency (Office Action, page 7).

As discussed above with respect to claims 1, 12, 26 and 28 Solution Brief 41 does not show or suggest selection circuitry that selects one of two values based on a control signal. Thus, Solution Brief 41 does not show or suggest these features defined by applicants' claims 22 and 30.

Therefore, Jaynes, WinSLAC and Solution Brief 41, whether taken alone or in combination, do not show or suggest all the features of applicants' claims 22 and 30. Accordingly, applicants respectfully submit that claims 22 and 30, and claims 21 and 36 that depend, directly or indirectly, from claim 22, are allowable.

Claims 24, 32 and 37

Claims 24, 32 and 37 were rejected under 35 U.S.C. § 103(a) as being obvious from Gorecki and Lu in view of WinSLAC and Solution Brief 41. This rejection is respectfully traversed.

Applicants' invention, as defined by independent claims 24 and 32, is directed to receiver circuitry and methods for adaptively equalizing a data signal. The receiver circuitry and methods include, *inter alia*, programmable circuitry that is programmed with a first value corresponding to a first sampling point location and outputs the first value and a control signal. Processing circuitry computes a second value corresponding to a second sampling point location and outputs the second starting value in parallel with the first starting value. Selection circuitry receives the control signal and the first and second values in parallel and selects one of the first and second values based on the control signal at the time the programmable circuitry is being programmed by configuration data.

The Examiner acknowledges that Gorecki and WinSLAC fail to show or suggest selection circuitry that selects one of the first and second values based on a control signal and relies on Solution Brief 41 to make up for this deficiency (Office Action, page 10-12).

As discussed above with respect to claims 1, 8, 26 and 27 Solution Brief 41 does not show or suggest selection circuitry that selects one of two values based on a control signal. Thus, Solution Brief 41 does not show or suggest these features defined by applicants' claims 24, 32 and 37. Lu was cited by the Examiner as allegedly showing other features of applicants' claims and does not make up for the deficiencies of Gorecki, Solution Brief 41 and WinSLAC relative to the rejection.

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Accordingly, applicants respectfully submit that claims 24, 32 and 37 are allowable.

Conclusion

For the reasons stated above, applicants respectfully submit that this application is in condition for allowance. Reconsideration and prompt allowance of this application are accordingly respectfully requested.

Respectfully submitted,

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